REMARKS

Claims 1-17 remain pending in the application.

The Applicants respectfully request the Examiner to reconsider earlier rejections in light of the following remarks. No new issues are raised nor is further search required as a result of the changes made herein. Entry of the Amendment is respectfully requested.

Claims 1-4 and 6-17 over Eaton in view of Feemster

In the Office Action, claims 1-4 and 6-17 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Pat. No. 3,924,245 to Eaton et al. ("Eaton") in view of U.S. Pat. No. 5,608,873 to Feemster et al. ("Feemster"). The Applicants respectfully traverse the rejection.

Claims 1-4, 6 and 7 recite a first **mailbox** portion addressably filling upward through to a highest physical address of a common memory, and a second **mailbox** portion addressably filling downward through to a lowest physical address of the common memory. Claims 8-17 recite a method and apparatus utilizing a shared memory comprising a maiilbox and allowing a first direction messages to utilize a dynamically allocated shared central portion of the shared memory addressably filling through to a second physical address end; and allowing a second direction messages to utilize the dynamically allocated shared central portion of a shared memory addressably filling through to a first physical address end.

The Examiner is apparently ignoring an very important feature of the claims, i.e., that it is the mailbox portion that grows in opposite directions. Neither Eaton nor Feemster disclose or suggest such a feature.

In the Response to the Arguments section of the Office Action, the Examiner alleges that Applicants argued (1) that Eaton teaches the use of a single processor and the memory is not shared (Office Action, page 10).

Although the Examiner alleges that Applicants argued Eaton teaches a single processor and a memory that is not shared, the Examiner goes on to acknowledge in the Office Action, page 10 that Applicants acknowledged

that Eaton discloses multiple processors that share a common memory, which is contradictory.

In the Response to the Argument section of the Office Action, the Examiner alleges that Applicants argued (2) that Eaton fails to disclose passage of data from one processing unit to another processing unit.

The Examiner is correct that Applicants argued Eaton fails to disclose passage of data from one processing unit to another processing unit because the Examiner alleges Eaton discloses a shared memory processor-to-processor mailbox between two processors (Office Action, page 2). However, the Examiner again contradicts the Examiners own assertion and acknowledges that Eaton is silent to passing data between multiple processors (Office Action, page 10). Instead, the Examiner relies on Feemster to allegedly disclose passing data between processors (Office Action, page 10).

The Examiner alleges that Applicants argued that (3) there is no motivation to combine the teachings of Eaton and Feemster (Office Action, page 10).

The Examiner acknowledges that "Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). (Office Action, page 11). However, the Examiner alleges that the Examiner does not suggest that the system of Eaton and Feemster would be physically combined to reach Applicants' claimed features, but stresses "the point is that the idea of common memory that addressably fills downward through to a lowest physical address of the common memory is taught by Eaton" (Office Action, page 11).

The Examiner is making the allegation that it would have been obvious to modify Eaton with the teachings of Feemster to arrive at the claimed features. However, the Examiner has still failed to provide a **single** suggestion or incentive why one ordinary skill in that art would have applied Eaton's teachings of a stack to a mailbox, as the Examiner acknowledged is required by In re Fine.

In fact, Eaton teaches away from passing data from one processor to another processor. Eaton discloses the use of two separate processing units with distinct separate memory areas and distinct separate registers (Eaton, col. 6, lines 42-54). Thus, the Examiner allegation of taking Eaton's relatively simple system having two processors **NOT INTERACTING** and modifying with features from a system using two processors that pass data between the processors is nonsensical. Eaton modified to pass data between processors fails to solves any shortcomings in Eaton that are needed for additional functionality. Without some suggestion or incentive to make the modification to Eaton, the Examiner is apparently using the Applicants' claimed features as a template to piece together the Eaton with Feemster. "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992).

The Examiner alleges that (4) the Applicants argued that the combination of Eaton and Feemster fails to teach first and second mailbox portions both defined in part over common memory addresses and the first mailbox addressing filling upward though a highest physical address of the common memory and second mailbox addressably filling downward through to a lowest physical address of the common memory (Office Action, page 10).

The Examiner alleges that the fact that Eaton does not use "mailbox" to represent the addressable memory areas that grows upward and downward does not affect the main idea of Eaton which is memory areas that grow/fills from opposite directions toward each other in a common memory (Office Action, page 11). The Applicants respectfully disagree.

The Examiner acknowledges that Eaton fails to disclose a "mailbox". However, a mailbox portion that grows in opposite directions is a very important feature **NOT** disclosed or suggested by either Eaton or Feemster. The piecemeal application of Eaton is improper: Eaton must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention (see MPEP 2141.02 at page 2100-95 (Rev. 1, Feb. 2000) (citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 22 USPQ 303 (Fed. Cir.

1983), cert. denied, 469 U.S. 851 (1984))). Eaton disclosed application of an addressable memory areas that grows upward and downward for separate distinct memory areas is **NOT** used to facilitate passing data between processors and a message between processors. In fact, Eaton teaches an addressable memory areas that grows upward and downward to keep data **SEPARATE** from two processors.

Thus, Eaton modified by Feemster would still result in an addressable memory area that grows upward and downward to keep data **SEPARATE** from two processors (Eaton), and when the processors need to pass data therebetween the mailbox features from Feemster would be used to facilitate such transfer.

Eaton modified by Feemster fails to disclose, teach or suggest a first **mailbox** portion addressably filling upward through to a highest physical address of a common memory, and a second **mailbox** portion addressably filling downward through to a lowest physical address of the common memory; and a method and apparatus utilizing a shared memory comprising a maiilbox and allowing a first direction messages to utilize a dynamically allocated shared central portion of the shared memory addressably filling through to a second physical address end; and allowing a second direction messages to utilize the dynamically allocated shared central portion of a shared memory addressably filling through to a first physical address end, as respectively recited by claims 1-4 and 6-17.

For at least all the above reasons, claims 1-4 and 6-17 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claim 5 over Eaton in view of Feemster and Frampton

In the Office Action, claim 5 was rejected under 35 U.S.C. §103(a) as allegedly being obvious over Eaton in view of Feemster, and further in view of U.S. Patent No. 5,802,351 to Frampton ("Frampton"). The Applicants respectfully traverse the rejection.

Claim 5 is dependent on claim 1, and is allowable for at least the same reasons as claim 1.

Claim 5 recites a first **mailbox** portion addressably filling upward through to a highest physical address of a common memory, and a second **mailbox** portion addressably filling downward through to a lowest physical address of the common memory.

As discussed above, Eaton in view of Feemster fails to disclose or suggest a first **mailbox** portion addressably filling upward through to a highest physical address of a common memory, and a second **mailbox** portion addressably filling downward through to a lowest physical address of the common memory, as recited by claim 5.

The Examiner relies on Frampton to allegedly make up for the deficiencies in Eaton in view of Feemseter to arrive at the claimed features. The Applicants respectfully disagree.

Frampton is relied on to disclose a share memory processor-to-processor mailbox between at least two processors is a dual port random access memory (Office Action, page 9). However, Frampton fails to disclose or suggest such a mailbox filling in opposite directions, i.e., a first **mailbox** portion addressably filling upward through to a highest physical address of a common memory, and a second **mailbox** portion addressably filling downward through to a lowest physical address of the common memory, as recited by claim 5.

Eaton in view of Feemster, and further in view of Frampton, still fails to disclose or suggest a mailbox that filling in opposite directions, i.e., a first **mailbox** portion addressably filling upward through to a highest physical address of a common memory, and a second **mailbox** portion addressably filling downward through to a lowest physical address of the common memory, as recited by claim 5.

For at least all the above reasons, claim 5 is patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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